O.P.Code: 19EC0409	R19	H.T.No.									

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech II Year II Semester Supplementary Examinations May/June-2024

LINEAR & DIGITAL IC APPLICATIONS

(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 60**

(Answer all Five Units **5 x 12 = 60** Marks)

		UNIT-I			
1	a	Describe about the block diagram of Op-Amp.	CO1	L2	6M
	b	Explain about the operation of sample and hold circuit with relevant Waveforms.	CO1	L1	6M
		OR			
2	a	Explain about the operation of sample and hold circuit with relevant Waveforms.	CO1	L1	6M
	b	Discuss about Schmitt trigger with neat sketches	CO1	L3	6M
		UNIT-II			
3	a	What is the principle operation of RC phase shift oscillator? Explain its operation.	CO2	L1	6M
	b	Explain the functional block diagram of 555 timers.	CO2	L5	6M
		OR			
4	a	Draw the circuit diagram of the wide Band-Reject Filter and explain its operation.	CO2	L2	6M
	b	Draw the frequency response curve for a band-pass filter.	CO2	L2	6M
		UNIT-III			
5		Draw and explain about R-2R DAC with an example.	CO3	L2	12M
		OR			
6		Draw the circuit diagram of Dual Slope ADC and explain its working with neat sketches.	CO3	L1	12M
		UNIT-IV			
7		Design the logic circuit and write VHDL program for the following function. F(X) = Σ A, B, C, D (0, 2, 5, 7, 8, 10, 13, 15) + d (1, 6, 11).	CO4	L6	12M
		OR			
8		Design a logic circuit for 4-bit parallel adder and write the VHDL code in structural style by considering full adder as a component.	CO4	L6	12M
		UNIT-V			
9	a	Design a 4 to 16 decoder with 74×138 IC's.	CO5	L6	6M
	b	Write a VHDL program for the above design.	CO5	L2	6M
		OR			
10		Design an 8 -bit serial in and serial out shift register and write a VHDL cod for it.	CO5	L6	12M

***** END *****